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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,438	12/15/2003	Andrew S. Hildebrant	10030775-1	3423

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2133	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/736,438	HILDEBRANT ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

GUY LAMARRE
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/20/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Response to the applicant's amendment dated 12/19/2006
- Claims 1-32 have been submitted for examination
- Claims 1-32 have been rejected

Response to Arguments

1. Applicant's arguments, see pages 7-12, filed on 12/19/2006, with respect to the rejection(s) of claims 1,12,17 and 28 under section 102(e0 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of Ishida et al. US patent no. 6661839 (Hereinafter Ishida) and further in view of Wang et al. US publication no. 2006/0242502 (Hereinafter Wang) and further in view of Testa et al. US patent no. 6205407 (Hereinafter Testa).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4-7,11,12, 16-18, 20-23, 27, 28 and 32 are rejected under 35

U.S.C. 102(e) as being anticipated by Ishida.

3. In regard to claim 1, Ishida teaches:

examining a test data file that includes a first plurality of data units corresponding to a first plurality of DUT pins (col. 2, line 55-56 in Ishida) and a second plurality of data units corresponding to a second plurality of DUT pins (col. 2, line 55-56 in Ishida);
compressing the first plurality of data units using a first compression technique; and compressing the second plurality of data units using a second compression technique (col. 2, lines 57-60 in Ishida).

4. In regard to claim 2, Ishida teaches:

determining a timing complexity for the first plurality of data units; and determining a timing complexity for the second plurality of data units(col. 3, lines 38-47 in Ishida).

5. In regard to claim 4, Ishida teaches:

wherein compressing the first plurality of data units by a predetermined compression rate requires more resources than compressing the second plurality of data units by the predetermined compression rate.
(Note: FIG. 2, in Ishida)

6. In regard to claim 5, Ishida teaches:
wherein the first plurality of data units have a different timing complexity than the second plurality of data units.
(Note; FIG. 6, reference character (65) and col. 3, lines 58-65 in Ishida)

7. In regard to claim 6, Ishida teaches:
wherein the first plurality of data units have a different vector data volume than the second plurality of data units.
(Note: FIG. 1 in Ishida)

8. In regard to claim 7, Ishida teaches:
wherein the first plurality of data units have more repetitive data patterns than the second plurality of data units.
(Note: FIG. 1 in Ishida)

9. In regard to claim 11, Ishida teaches:

wherein at least one processor operating in a first timing domain enables the first plurality of data units to be provided to the first plurality of DUT pins, and at least one processor operating in a second timing domain enables second plurality of data units to be provided to the second plurality of DUT pins, wherein the second timing domain is different from the first timing domain.

(Note; FIG. 112, reference characters (588), (592) & (593) in Ishida)

10. Claim 12 is rejected for the same reasons as per claim 1.

11. Claims 16 and 32 are rejected for the same reasons as per claims 5, 6 and 7.

12. In regard to claim 17, Ishida teaches:

memory configured to store a test data file that includes a first plurality of data units corresponding to a first plurality of DUT pins and a second plurality of data units corresponding to a second plurality of DUT pins; and a processor operative to: compress the first plurality of data units using a first compression technique; and compress the second plurality of data units using a second compression technique.

(Note: Figures (112) and (113) in Ishida)

13. Claim 18 is rejected for the same reasons as per claim 2.
14. Claim 20 is rejected for the same reasons as per claim 4.
15. Claim 21 is rejected for the same reasons as per claim 5.
16. Claim 22 is rejected for the same reasons as per claim 6.
17. Claim 23 is rejected for the same reasons as per claim 7.
18. Claim 27 is rejected for the same reasons as per claim 11.
19. Claim 28 is rejected for the same reasons as per claim 17.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

20. Claims 3, 8, 9, 13,14, 19, 24, 25, 29 and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida as applied to claim 1 above, and further in view of Wang et al. US publication no. 2006/0242502 (Hereinafter Wang).

21. In regard to claim 3, Ishida substantially teaches all the limitations in claim 1. However, Ishida does not teach:

wherein the first plurality of data units corresponds to clock signals and the second plurality of data units corresponds to non-clock signals.

Wang in an analogous art that teaches method and apparatus for broadcasting SCAN patterns in a random access SCAN based integrated circuit teaches:

wherein the first plurality of data units corresponds to clock signals (FIG. 1, reference character (111) in Wang) and the second plurality of

data units corresponds to non-clock signals (FIG. 1, reference character (113) in Wang).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Ishida that comprise comprising of test data files with the teaching of Wang.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need to cover more faults per scan test pattern.

22. In regard to claim 8, Wang teaches:

wherein the first plurality of DUT pins are clock-pins (FIG. 1, reference character (111) in Wang) and the second plurality of DUT pins are non-clock-pins (FIG. 1, reference character (113) in Wang).

23. In regard to claim 9, Wang teaches:

formatting the first plurality of data units independently from the second plurality of data units.
(Note: FIG. 6 in Wang)

24. Claims 13 and 25 and 29 are rejected for the same reasons as per claim 9.

25. Claim 14 is rejected for the same reasons as per claim 3.

26. Claim 19 is rejected for the same reasons as per claim 3.

27. Claims 24 and 30 are rejected for the same reasons as per claim 8.

28. Claims 10, 15, 26 and 31are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida as applied to claim 1 above, and further in view of Testa et al. US patent no. 6205407 (Hereinafter Testa).

29. In regard to claim 10, Ishida substantially teaches all the limitations in claim 1. However Ishida does not teach:

wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.

Testa in an analogous art that teaches system and method for generating test program codes teaches:

wherein the test data file is one of a STIL (standard test interface language) file and a WGL (waveform generation language) file.
(Note: col. 9, lines 5-35 in Testa)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Ishida that comprise comprising of test data files with the teaching of Testa.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need to cover more faults per scan test pattern.

30. Claims 15, 26, 31 are rejected for the same reasons as per claim 10.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

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